

Roll No. ....

**24487**

**B.Tech. 7th Sem.  
(Computer Science Engineering)  
Examination-May, 2013**

**ADVANCED COMPUTER ARCHITECTURE**

**Paper CSE-401-F**

**Time : 3 hours**

**Max. Marks : 100**

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard will be entertained after the examination.

**Note : Question No. 9 is compulsory. Attempt five questions in total selecting one question from each of the four Section.**

**SECTION - A**

1. (a) Compare hardwired control with micro-programmed control. 6
- (b) WAP in assembly language to add a constant value #X to each element of an array in L/S and R/M arch mode. 14

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(1)

[ Turn Over

2. (a) A  $2.3 \text{ cm}^2$  die can be fabricated on a 15 cm wafer at a cost of ₹5,000, or on a 20 cm wafer at the cost of ₹6,000. Compare the effective cost per die for defect densities of 0.4 defect/ $\text{cm}^2$  and 0.9 defects per  $\text{cm}^2$ . 15
- (b) Briefly explain clock skew and cycle quantization. 5

### SECTION - B

3. (a) Explain various Cache write policies. 10
- (b) In two level Cache system, we have 10
- L1 size 8 KB with 4w set assoc, 16B lines (WTNWA)
  - L2 size 64 KB, direct mapping, 64B lines and CBWA.

Suppose the miss in L1, hit in L2 delay in 3 cycles and the miss in L1, miss in L2 delay is 10 cycles. The processor makes 1.5 reference/1 :

- (a) What are L1 and L2 miss rates ?
- (b) What is the expected CPI loss due to Cache misses.



4. (a) Explain fully associative mapping scheme for Cache memory. 10  
(b) Explain write assembly Cache, split Cache in detail. 10

#### SECTION - C

5. Explain Hellerman's Strecker's and Rau's memory model in detail. 20  
6. Explain open and closed queue models in detail. 20

#### SECTION - D

7. Why memory coherence is essential in shared memory multiprocessors. Explain the various approaches and protocols to maintain this. 20  
8. Write notes on : 20  
(a) Partitioning  
(b) Vector processor  
(c) VLIW.

**9. Compulsory question :**

(a) Define state, cycle, command process.

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(b) Describe locality of reference and its type.

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(c) How address space is assigned to different memory modules ?

5

(d) Explain the various run-time scheduling techniques.

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